High-performance Multi-queue Buffers For VLSI Communication Switches (Report. University Of California, Los Angeles. Computer Science Dept)

By Yuval Tamir

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High Performance multi-queue buffers for VLSI allocated multi-queue (DAMQ) buffer, key to the ability of multicomputers to achieve high performance.

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High-performance multiqueue buffers for VLSI communication switches - Co mputer Architecture, 1988. Conference Proceedings. 15th Annual Internati onal Symposium on

Patent US8180897 - Apparatus and method for -
An apparatus in one embodiment handles service requests over a network, wherein the network utilizes a protocol. In this aspect, the apparatus includes: a network

Lock-free, Thread Based Log Buffer Implementation, -
Sep 28, 2014 for debugging high performance multi-threaded log buffer implementation, for debugging high performance multi free circular array queue.

Patent US6766381 - VLSI network processor and -
A network processor useful in network switch apparatus and methods of operating such a processor in which data flow handling and flexibility is enhanced by the

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Buffer insertion is an important technique used to achieve timing closure in high performance VLSI designs. As the number of buffers in ASIC designs has increased

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for the dynamically allocated multi-queue A VLSI Self-Compacting Buffer for DAMQ Communication The proposed implementation provides a high-performance

Patent US8028115 - File system adapter for -
A file system adapter card that may be plugged into a host computer system for providing hardware-based file system accesses outside the purview of a host operating

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